AMENDMENT TO THE CLAIMS

Please amend claims 1, 16 and 27 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

forming, by removing material from an upper surface of a substrate, a p-type field-effect-transistor (PFET) channel and a n-type field-effect- transistor (nFET) channel in a the substrate;

providing a first layer of material within the pFET channel having a lattice constant different than the lattice constant of the substrate;

providing a second layer of material within the nFET channel having a lattice constant different than the lattice constant of the substrate, the second layer of material being different from the first layer of material;

forming an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate such that a stress component is created within the pFET channel and the nFET channel.

Claim 2. (Original) The method of claim 1, wherein the pFET channel and the nFET channel are formed simultaneously.

Claim 3. (Original) The method of claim 1, wherein the pFET channel and the nFET channel are formed separately.

Claim 4. (Original) The method of claim 1, wherein the first layer of material is SiGe having a content of Ge approximately greater than 25% in ratio to Si.

Claim 5. (Original) The method of claim 4, wherein the first layer of material creates a tensile stress within the epitaxial semiconductor layer of greater than 3 GPa.

Claim 6. (Original) The method of claim 1, wherein the second layer of material is SiGe.

Claim 7. (Original) The method of claim 6, wherein the second layer of material creates a tensile stress within the epitaxial semiconductor layer within the nFET channel.

Claim 8. (Original) The method of claim 1, wherein the first layer of material is Si:C.

Claim 9. (Original) The method of claim 1, further comprising the steps of:

forming a gate oxide structure over the epitaxial semiconductor layer; and

forming extensions and a drain region and a source region in the substrate on sides of the gate oxide structure.

Claim 10. (Previously Presented) The method of claim 1, wherein the forming of the nFET and pFET channels includes etching an Si layer of the substrate to approximately a depth of about 200Å to 400Å.

Claim 11. (Original) The method of claim 1, wherein:

the first layer of material is formed by placing a hard mask over the nFET channel and growing the first layer of material within the pFET channel; and

the second layer of material is formed by placing a hard mask over the pFET channel and growing the second layer of material within the nFET channel.

Claim 12. (Original) The method of claim 1, further comprising forming shallow trench structures within the substrate.

Claim 13. (Original) The method of claim 1, wherein the first layer of material and the second layer of material are grown to a height about 100 Å to 300 Å.

Claim 14. (Previously Presented) The method of claim 1, wherein the substrate is a layer of silicon on insulator.

Claim 15. (Original) The method of claim 1, wherein the first layer of material and the second layer of material are both SiGe material, having a larger Ge percentage than approximately 25% to 30% to apply for the pFET.

Claim 16. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (PFET) channel and a n-type field-effect-transistor (nFET) channel by etching an upper surface ~~in~~ of a substrate;

providing a first layer of material within the pFET channel having a lattice constant different than the lattice constant of the substrate;

providing a second layer of material within the nFET channel having a lattice constant different than the lattice constant of the substrate, the second layer of material being different from the first layer of material; and

forming an epitaxial semiconductor layer over the first layer of material in the pFET channel and the second layer of material in the nFET channel, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate thus creating a stress component opposite to that of the first layer of material within the pFET channel and the second layer of material within the nFET channel.

Claim 17. (Original) The method of claim 16, wherein the pFET channel and the nFET channel are formed simultaneously.

Claim 18. (Original) The method of claim 16, wherein the pFET channel and the nFET channel are formed separately.

Claim 19. (Original) The method of claim 16, wherein the first layer of material is Si:C and the second layer of material is SiGe.

Claim 20. (Original) The method of claim 19, wherein:

the first layer of material creates a compressive stress within the epitaxial semiconductor layer within the pFET channel;

and the second layer of material creates a tensile stress within the epitaxial semiconductor layer within the nFET channel.

Claim 21. (Previously Presented) The method of claim 16, further comprising the steps of:

forming a gate oxide structure over the epitaxial semiconductor layer; and

forming extensions and a drain region and a source region in an Si layer of the substrate on sides of the gate oxide structure.

Claim 22. (Original) The method of claim 16, wherein:

the first layer of material is formed by placing a hard mask over the nFET channel and growing the first layer of material within the pFET channel; and

the second layer of material is formed by placing a hard mask over the pFET channel and growing the second layer of material within the nFET channel.

Claims 23-26. (Canceled)

Claim 27. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

~~forming~~ etching an upper layer of a substrate a p-type field-effect-transistor (PFET) channel and a n-type field-effect- transistor (nFET) channel ~~in a substrate~~;

providing a layer of Si:C within the pFET channel having a lattice constant different than the lattice constant of the substrate;

providing a layer of SiGe within the nFET channel having a lattice constant different than the lattice constant of the substrate;

forming an epitaxial semiconductor layer over the layers of Si:C and SiGe in the pFET and the nFET channels, the epitaxial semiconductor layer having substantially a same lattice constant as the substrate such that different stress components are created within the pFET channel and the nFET channel.